Reg.No. \_\_\_\_\_\_\_\_\_\_\_\_



**End Semester Examination – Nov/Dec – 2018**

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| **Code :** | **18EI3001** | **Duration :** | **3hrs** |
| **Sub. Name :** | **ADVANCED EMBEDDED SIGNAL PROCESSORS** | **Max. marks :** | **100** |

**ANSWER ANY FIVE QUESTIONS (5 x 16 = 80 Marks)**

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| **Q. No.** | **Sub Div.** | **Questions** | **Course**  **Outcome** | **Marks** |
| 1. | a. | Discuss the pros and cons of Digital Signal Processing. | CO1 | 7 |
| b. | Discus the FIR filter hardware implementation scheme with single multiplier/adder. | CO1 | 7 |
| c. | Write the procedure to obtain equivalent structure. | CO1 | 2 |
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| 2. | a. | Explain briefly the difference between von Newmann architecture and Harvard architecture for the computer. Which architecture is preferred for DSP’s and why? | CO2 | 7 |
| b. | Explain the operation of TDM serial ports in P-DSPs with a neat block diagram. | CO2 | 7 |
| c. | VLIW architecture differs from conventional PDSP in which of the  following aspects: (i) Instruction cache (ii) No. of functional units  (iii) Use pipelining (iv) A single word fetched from memory has a  no. of instructions. | CO2 | 2 |
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| 3. | a. | Discuss with a block diagram the role played by ARAU in TMS320c5x PDSP | CO3 | 6 |
| b. | Write a C5x assembly level program for the implementation of FIR filter using MAC instruction. ( Assumey[m] = { 3,4,5}, x[n] = {1,2,3,2,1 } ) | CO3 | 10 |
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| 4. | a. | Draw and explain the internal architecture of TMS320C54X PDSP. | CO4 | 8 |
| b. | Discuss the TMS320C6x assembly programs for Serial/Partially Parallel/ Fully Parallel FIR filter implementation. | CO4 | 8 |
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| 5. | a. | Explain with block diagram how 5-Input Functions can be implemented using two LUTs | CO5 | 8 |
| b. | Discuss Xilinx XC3000 Configurable Logic Block (CLB) | CO5 | 8 |
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| 6. | a. | Draw the table showing the content of the instruction pipeline of TMS320C5x & the content of ARP, AR6, TREG0, PREG, ACC registers when each of the sequence of 1-word instructions of the following program is executed. Initial content of memory locations 60h = 10h, 61h = 3h & 62h = 6h.  **ADD \*+**  **SAMM TREG0**  **MPY \*+**  **SQRA \*+, AR2** | CO3 | 8 |
| b. | Discuss the pipelining implemented in TMS320C54x and bring out how it is different from that of TMS320C5x processor. | CO4 | 8 |
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| 7. | a. | Explain with examples the Block Move instructions of TMS320C5x processor using various addressing modes. | CO3 | 5 |
| b. | Explain how the Register-indirect Addressing is implemented in TMS320C5x processor with   1. Modulo address arithmetic 2. Bit Reversal | CO3 | 4  4 |
| c. | Explain the salient features of Barrel shifter used in PDSPs | CO2 | 3 |
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| **COMPULSORY QUESTION (1 x 20 = 20 Marks)** | | | | |
| 8. | a. | Compare the Digit Serial Computation and Bit Serial computation architecture used in FPGA for DSP applications. | CO6 | 10 |
| b. | Explain with neat block diagram the MAC Implementation using Distributed Arithmetic in FPGA. | CO6 | 10 |